IN THE SPECIFICATION:

Please amend the specification as follows:

Please delete in their entirety the paragraphs beginning on page 2, at prenumbered lines 10, 17 and 24, respectively, and replace the following new paragraphs therefor:

In accordance with a first aspect of the invention there is provided a process for making an integrated circuit package comprising the steps of: providing a substrate having a chip-attaching surface; applying an A-stage liquid paste on the chip-attaching surface of the substrate, the A-stage liquid paste including a thermosetting material and a solvent; heating the substrate to remove the solvent of the A-stage liquid paste in a manner that the A-stage liquid paste is transformed into a dry B-stage film layer; attaching a chip to the chip-attaching surface of the substrate by the B-stage film layer, the B-stage film layer being maintained in a partially cured condition; electrically connecting the chip with the substrate having the B-stage film layer; and forming a molding compound on the chip-attaching surface of the substrate, the packing pressure for the molding compound being larger than the chip-attaching pressure in a manner that the partially-cured B-stage film layer re-bonds the chip to improve effective chip-bonding area.

As the packing pressure for the molding compound is larger than the chip-attaching pressure, the B-stage film layer can further closely re-bond the chip for improving effective chip-bonding area in molding step.

In a second aspect of the invention, there is provided a process for making an integrated circuit package comprising the steps of: providing a substrate having a chip-attaching surface; applying an A-stage liquid paste on the chip-attaching surface of the substrate; heating the substrate to transform the A-stage liquid paste into a B-stage film layer, the B-stage film layer having a glass transition temperature (Tg); attaching a chip to the chip-attaching surface of the substrate, the substrate is heated being higher than the glass transition temperature (Tg) of the B-stage film layer to make the B-stage film layer adhere the substrate and the chip, and the B-stage film layer being maintained in a partially-cured condition; electrically

connecting the chip with the substrate having the B-stage film layer; and forming a molding compound on the chip-attaching surface of the substrate, the packing pressure for the molding compound being larger than the chip-attaching pressure in a manner that the partially-cured B-stage film layer re-bonds the chip to improve effective chip-bonding area.

As the B-stage film layer has a glass transition temperature (Tg) lower than chip-attaching temperature and has a thermosetting temperature lower than thermosetting temperature of the molding compound, the B-stage film layer can be closely compressed between the chip and the substrate to remove gaps or voids in the molding step.

The packing pressure for the molding compound is preferably approximately 6.9 MPa (1000psi) to 10.3 MPa (1500psi), which is larger than the chip-attaching pressure, so that the B-stage film layer can be closely compressed to re-bond the chip in order to improve the effective chip-bonding area. The heating temperature in the molding step is preferably approximately 150°C to 200°C, which is higher than the fully curing temperature of the B-stage film layer, so as to cure the B-stage film layer and the molding compound simultaneously.

Paragraph beginning on page 6, at prenumbered line 7, has been amended as follows:

Finally, a showed in Fig. 3 and Fig. 4F, the molding step 106 is performed. The molding step 106 includes a filling sub-step and a packing sub-step for forming a molding compound 150 on the substrate 110 by molds 151,152. In the filling sub-step, the substrate 110 with the attached chip 130 and the B-stage film layer 122 is placed inside the mold cavity formed by an upper mold 151 and a lower mold 152. A molding compound 150 is filled into the mold cavity under a filling pressure until filling over 80 vol% of the mold cavity. The molding compound 150 includes thermosetting resin, curing agent, silicate filler, releasing wax and a few coloring agent. In the packing sub-step, the packing pressure higher than the filling pressure is applied to the molding compound 150 inside the mold cavity to remove voids in the molding compound 150 and the voids in the B-stage film layer 122. The packing

pressure is ~~about 1000psi ~ 15000psi~~ preferably 1000ps (6.9 MPa) to 1500psi (10.2 MPa), which is larger than the chip attaching pressure mentioned in the chip attaching step 104. After completing the chip attaching step 104 and the electrically connecting step 105, the B-stage film layer 122 is still in partially curing condition and can be deformed suitably. The B-stage film layer 122 is closely compressed under the high packing pressure for the molding compound 150, so that the voids and gaps inside the B-stage film layer 122 will be removed so as to improve effective chip-bonding area between the chip 130 and the substrate 110. Preferably, the heating temperature in the molding step 106 for curing the molding compound 150 is about 150°C ~ 200°C that matches the fully curing temperature of the molding compound 150, so that the B-stage film layer 122 and the molding compound 150 are cured simultaneously. After the molding step 106, the B-stage film layer 122 is transformed into the C-stage film layer 123 (as showed in Fig. 5) to be a stable fixed film layer. In this embodiment, a step follows the molding step 106 to plant a plurality of solder balls 160 on the surface-mounting surface 113 of the substrate 110, then the substrate 110 is diced and separated to construct a ball grid array (BGA) package with excellent reliability. The packaging process for improving effective chip-bonding area of the present invention is suitable for various packages, especially for chip scale package (CSP). The B-state film layer 122 won't contaminate the connect pads 112 of the substrate 110, so that the connect pads 112 may be arranged to be closely near to the chip 130. Advantageously, after dicing the substrate 110 to form separate integrated circuit package, the chip-attaching surface 111 of the substrate 110 is not larger than 1.5 times the active surface 132 of the chip 130 in area so as to form a chip scale package (CSP).